SET-C

Instructions: 1) Each question is of 10 marks.

2) Attempt the question in your handwritten self and upload the solution on UMS before the date of submission in PDF format

3) Please mention your details on the top of each page: Name, Reg. No., Class Roll no., set no.

1. If you weren't allowed to use multiplexers, can you realize the data transfer system hardware in any other manner? If yes, Can you implement and show how and what can be used for 2 registers with 3 bits inside them.

2. a).   Starting from an initial value of R= 11011100 determine the sequence of binary values in R after performing a logical shift-right, followed by a circular shift right, followed by a logical shift left , followed by a circular shift left, followed by an arithmetic shift right , followed by an arithmetic shift left , followed by a circular shift right ,followed by a logical shift right and followed by a arithmetic shift right?   (b) Draw shifter diagram. Along with truth table and explanation .

3. If 8 bits register R=01011011, Perform

(I) R<—-ashr R ,

(II) R<—-ashl R , and Determine decimal equivalent values forR, ashr R and ashl R

(III) State whether there is overflow or not in case of ashl R

(IV) R<—- cir R

(v) R<—— shr R

(VI) R<—— R-1

(VII) R<—— R+1

(VIII) R<—— R'

(IX) R<—— shl R

(X) R<—— cil R